The Claims:

Listing of Claims:

1. (Previously Presented) A method for processing data using a plurality of processing engines, the method comprising:

processing first data associated with an older control record in a first processing engine;

enabling a first interrupt indicator in the older control record when the processing of the first data is completed;

processing second data associated with a younger control record in a second processing engine;

enabling a second interrupt indicator in the younger control record when the processing of the second data is completed; and

moving the second interrupt indicator associated with the younger control record onto the first interrupt indicator associated with the older control record if processing of the second data completes before processing of the first data.

2. (Original) The method of claim 1, wherein the first processing engine is a public key engine.

3. (Previously Presented) The method of claim 1, wherein moving the second interrupt indicator comprises determining that the second interrupt indicator is enabled.

4. (Previously Presented) The method of claim 1, wherein moving the second interrupt indicator comprises delaying the generation of an interrupt associated with the younger control record.

5. (Canceled)

6. (Previously Presented) The method of claim 4, wherein moving the second interrupt indicator comprises setting the second interrupt indicator associated with the younger control record to disabled.

7. (Previously Presented) The method of claim 6, wherein moving the second interrupt indicator further comprises setting the first interrupt indicator associated with the older control record to enabled.

8. (Original) The method of claim 1, wherein the older control record comprises a reference to data.

9. (Original) The method of claim 8, wherein the older control record comprises a reference to an operation to be performed on data.

10. (Original) The method of claim 1, further comprising writing processed data to memory associated with a host.

11. (Previously Presented) The method of claim 10, wherein the host is an external processor coupled to the processing engines.

12. (Previously Presented) The method of claim 11, wherein the external processor is coupled to the processing engines through a scheduler.

13. (Original) The method of claim 12, further comprising generating an interrupt when processing of the older control record has been completed.

14. (Original) The method of claim 13, wherein the external processor reads the processed data when the interrupt is generated.

15. (Previously Presented) A cryptography accelerator, comprising:

an interface coupled to an external processor and memory associated with the external processor;

a first processing engine coupled to the interface, the first processing engine configured to receive a first control record from the external processor;

a second processing engine coupled to the interface, the second processing engine configured to receive a second control record from the external processor;

a history buffer containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record, wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record.

16. (Original) The cryptography accelerator of claim 15, wherein the first processing engine is a public key engine.

17. (Previously Presented) The cryptography accelerator of claim 15, wherein the history buffer is configured to collapse the first interrupt indicator associated with the first control record onto the second interrupt indicator associated with the second control record when the first interrupt indicator is enabled.

18. (Previously Presented) The cryptography accelerator of claim 17, wherein collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises delaying the generation of an interrupt associated with the first control record.

19. (Canceled)

20. (Original) The cryptography accelerator of claim 18, wherein collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the first interrupt indicator associated with the first control record to disabled.

21. (Original) The cryptography accelerator of claim 20, wherein collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the second interrupt indicator associated with the second control record to enabled.

22. (Original) The cryptography accelerator of claim 15, wherein the second control record comprises a reference to data.

23. (Original) The cryptography accelerator of claim 22, wherein the second control record comprises a reference to an operation to be performed on data.

24. (Previously Presented) The cryptography accelerator of claim 23, wherein the external processor is coupled to the processing engines through a scheduler.

25. (Original) The cryptography accelerator of claim 24, wherein an interrupt is generated when processing of the second control record has been completed.

26. (Original) The cryptography accelerator of claim 25, wherein the external processor reads the processed data when the interrupt is generated.

27. (Previously Presented) A method for handling interrupts, the method comprising:

receiving a first data block associated with a first interrupt indicator set to enabled, wherein the first interrupt indicator is configured to cause the generation of a first interrupt upon completion of processing of the first data block;

processing the first data block using a first processing engine;

receiving a second data block associated with a second interrupt indicator set to enabled, wherein the second interrupt indicator is configured to cause the generation of a second interrupt upon completion of processing of the second data block;

processing the second data block using a second processing engine;

determining if any of the first or second interrupt indicators is enabled;

if the second interrupt indicator is enabled and the processing of the first data block is not completed, generating a single interrupt upon completion of processing of the first data block.

28. (Original) The method of claim 27, wherein the first and second processing engines are public key engines.

29. (Original) The method of claim 27, wherein the first data block is referenced in a first control record.

30. (Original) The method of claim 29, wherein the first control record contains information on an operation to perform on the first data block.

31. (Previously Presented) The method of claim 27, wherein the single interrupt is generated after processing of the first data block is completed.

32. (Original) The method of claim 27, wherein the first interrupt indicator associated with the first data block is collapsed onto the second interrupt indicator associated with the second data block.

33. (Original) The method of claim 32, wherein collapsing the first interrupt indicator comprises setting the first interrupt indicator to disabled.

34. (Original) The method of claim 33, wherein collapsing the first interrupt indicator comprises setting the second interrupt indicator to enabled.

35. (Previously Presented) A cryptography device, comprising:

means for receiving a first data block associated with a first interrupt indicator set to enabled, wherein the first interrupt indicator is configured to cause the generation of a first interrupt upon completion of processing of the first data block;

means for processing the first data block using a first processing engine;

means for receiving a second data block associated with a second interrupt indicator set to enabled, wherein the second interrupt indicator is configured to cause the generation of a second interrupt upon completion of processing of the second data block;

means for processing the second data block using a second processing engine;

means for determining if any of the first or second interrupt indicators is enabled;

means for generating a single interrupt upon completion of processing of the first data block, if the second interrupt indicator is enabled and the processing of the first data block is not completed.

36. (Original) The cryptography device of claim 35, wherein the first and second processing engines are public key engines.

37. (Original) The cryptography device of claim 35, wherein the first data block is referenced in a first control record.

38. (Original) The cryptography device of claim 37, wherein the first control record contains information on an operation to perform on the first data block.

39. (Previously Presented) The cryptography device of claim 35, wherein the single interrupt is generated after processing of the first data block is completed.

40. (Original) The cryptography device of claim 35, wherein the first interrupt indicator associated with the first data block is collapsed onto the second interrupt indicator associated with the second data block.

41. (Original) The cryptography device of claim 40, wherein collapsing the first interrupt indicator comprises setting the first interrupt indicator to disabled.

42. (Original) The cryptography device of claim 41, wherein collapsing the first interrupt indicator comprises setting the second interrupt indicator to enabled.